Backside Illuminated Hybrid FPA achieving Low Cross-Talk combined with High QE

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Backside-thinned fully-hybrid CMOS imagers (Figure 1) possessing excellent imaging properties have been previously reported † [1, 2, 3]. An excellent quantum efficiency (QE) greater than 80% (400nm—800nm) was achieved (Figure 2), thanks to optimized backside illuminated detector and anti-reflective coating [4]. Innovative process techniques to handle the thin wafers and to achieve high pixel & bump yields (99.98% & 99.93% respectively) were also reported [2].
Although excellent in terms of sensitivity (QE) [4], backside illuminated imagers (BSI) generally suffer from larger electrical inter-pixel cross-talk (or charge-dispersion). When employing thick bulk silicon to maximize red response, the natural inverse relationship between QE and cross-talk results in large cross-talk in particular for blue light (for BSI). By using a dopant graded epitaxial substrate, an internal electric field can be generated which pushes generated charge carriers to the collection node.
Initially, a non-optimal "stepped" profile (Figure 3) was used to emulate this effect, though measurements showed that cross-talk remained high [1]. The effective electric field was too low to have a significant impact on cross-talk. Nevertheless, in parallel, the use of high aspect ratio (1:50) trenches to physically separate the pixels [3] was explored. This resulted in a dramatic reduction of cross-talk (below the detection limit of the measurement method), but also in an overall attenuated QE most pronounced in the shorter wavelength regions.
In a second generation of devices we undertook the exercise of solving the cross-talk problem by a two-pronged approach, both of which work on increasing the charge guiding electric field:

A) Realize an optimized graded epitaxial profile
B) Employ a fully-depleted version using high-resistivity (n-and p-type) silicon substrates

An optimal epitaxial substrate was engineered and subsequently realized with the goal of achieving a profile with a "slope" as steep as possible to maximize the internal electric field. On this starting material, 1 Mpixel, 22.5 µm pitch hybrid diodes were processed at imec and hybridized on a dedicated CMOS readout [2]. These sensors are being characterized.
The cross-talk (i.e. charges generated at one pixel but collected by surrounding pixels) is experimentally mapped by means of a single pixel illumination technique using a focused laser and shown in Figure 4. Compared to the "stepped" profile (cross-talk~89%), there is a drastic improvement for the new profile (cross-talk~17%). Formulated in cross-talk to the nearest neighbor this comes down to ~2%, limited by the laser spot size of the characterization technique. Naturally, the high aspect ratio trenches (Figure 5) provide the best possible cross-talk performance.
In parallel, devices have been designed and fabricated on high-resistivity (~ 3×10^{12} at/cm^3) n-and p-type silicon substrates. Specific technology was developed to enable in-house handling of high resistivity substrates. These wafers were also thinned in order to easily achieve full depletion with an adequate electric field around 2V. These sensors utilize a commercial CTIA (Charge Trans-impedance Amplifier) read-out IC (ROIC). The hybridized and packaged imager is shown in Figure 6. More detailed characterization results on these devices will be presented.

References

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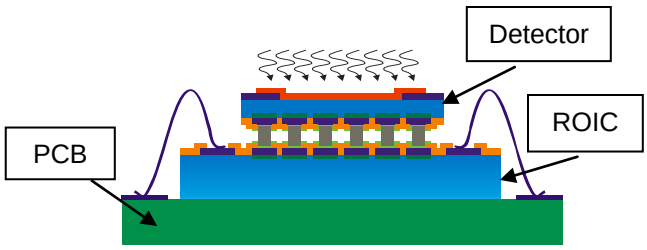
2. K. De Munck, et al., "High performance hybrid and monolithic backside thinned CMOS imagers realized using a new integration process", proc. IEEE International Electron Devices Meeting, pp:139-142, 2006, San Francisco, US
3. K. Minoglou, et al., "Reduction of electrical crosstalk in hybrid backside illuminated CMOS imagers using deep trench isolation", proc. IEEE International Interconnect Technology Conference, pp: 129-131, June 2008, San Francisco
4. Koen De Munck et al., "Backside thinned CMOS imagers with high broadband quantum efficiency realized using a new integration process", Electronics Letters, vol. 44, no. 1, pp: 50-52, 2008

† Development of these imagers was done in the frame of an ESA funded project (AO/1-3970/02/NL/EC).



Hybridization: pixel- wise Indium bump connection between ROIC and flipped thinned detector array

Figure 1 Conceptual drawing of a fully hybridized imager

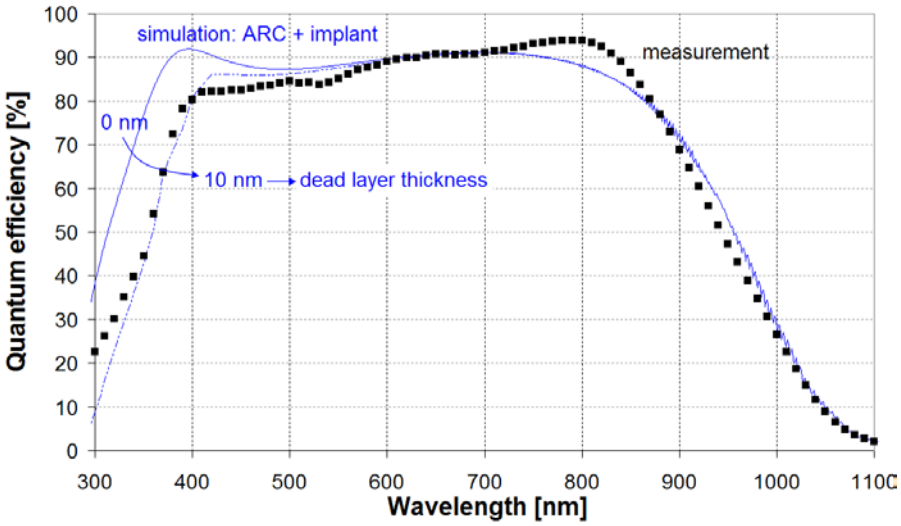


Figure 2 Measured and simulated QE after backside passivation and ARC

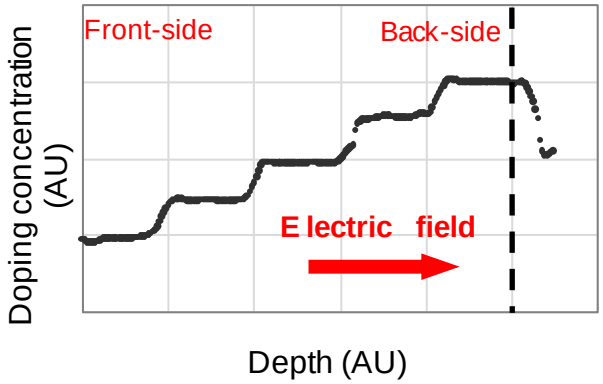


Figure 3 Initial "stepped" EPI-profile. This profile results in large cross-talk

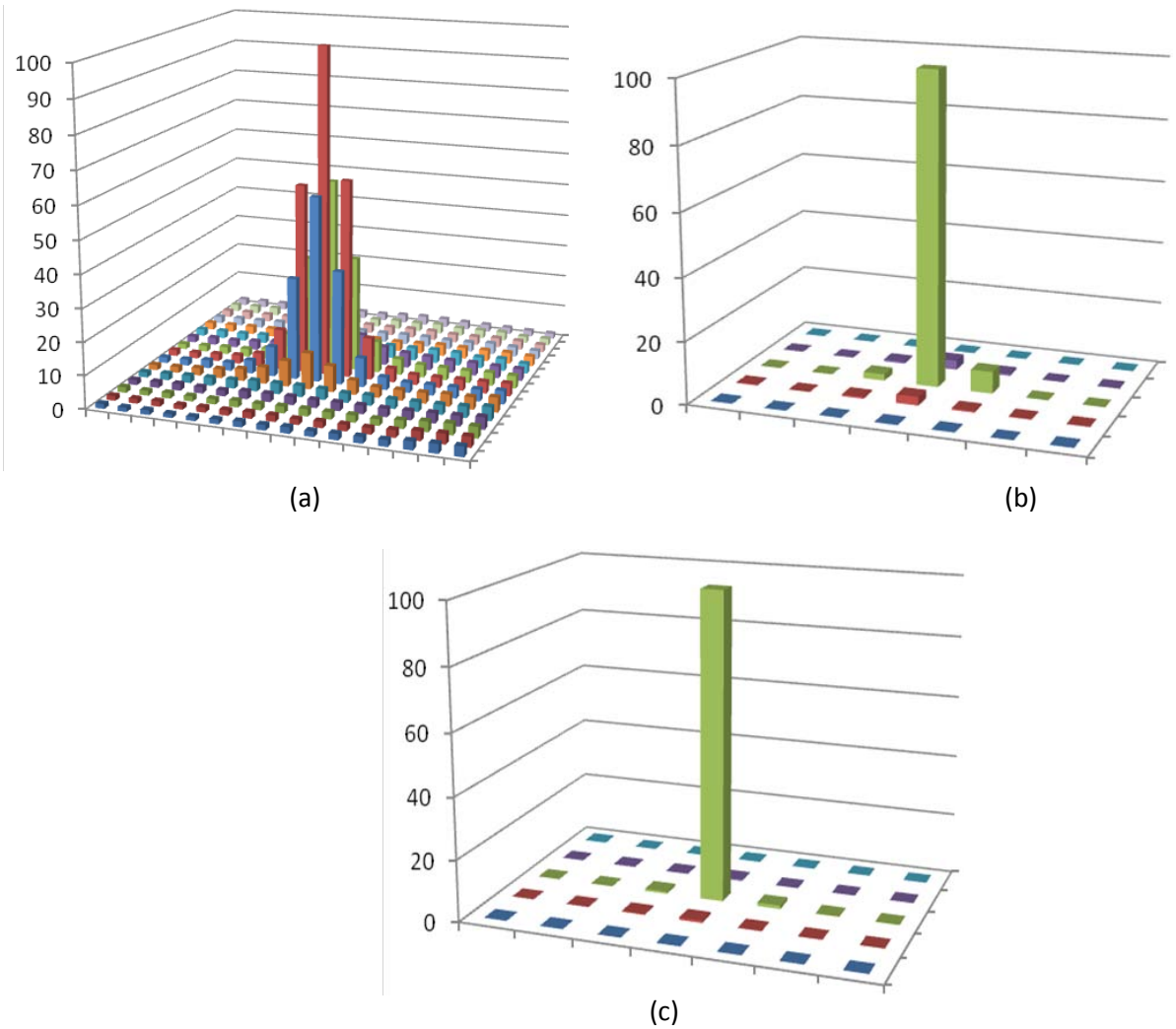


Figure 4 Cross talk measured with the single-spot illumination technique and normalized to the central pixel a) previous "stepped" profile; b) current profile; c) sensors with pixel separating trenches

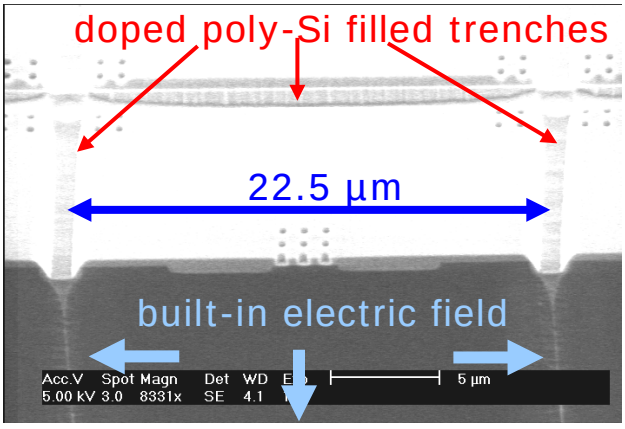


Figure 5 Top view and cross section FIB of one 22.5µm pixel surrounded by trenches

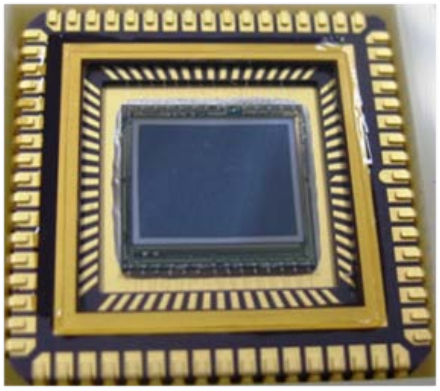


Figure 6 The fully-depleted sensor array bump-bonded to an CTIA-based ROIC and packaged